PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No. 8661
Tomoharu Tanaka et al.	Group Art No. 2824
Serial No.: 10/656,139	Examiner: LE, Vu Anh
Filed: September 8, 2003	Docket No: 001701.00676
For: Non-Volatile Semiconductor Memory Device Adapted To Store A Multi-Valued Data In A Single Memory Cell	

INFORMATION DISCLOSURE STATEMENT

Mail Stop 313(c)
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attention: Karen Creasey
Via Facsimile
571-273-0025

Sir:

Pursuant to 37 C.F.R. §1.56 and in compliance with 37 C.F.R. §1.97, Applicants submit herewith Form PTO/SB/08, identifying information for consideration by the Examiner. A copy of the item of information is enclosed.

The undersigned certifies under 37 C.F.R. § 1.704(d) that each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counter part application and that this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this statement.

Applicants do not waive any rights to take appropriate action to establish patentability over the listed document should it be applied as a reference against the claims of the present application.

Consideration of the cited information and making the same of record in the prosecution of the above-noted application are respectfully requested. Should the Patent and Trademark Office determine that a fee is required, please charge our Deposit Account No. 19-0733.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: February 10, 2005

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete If Known	
Application Number	0/656,139
Filing Date	September 8, 2003
First Named Inventor	Tomoharu Tanaka et al.
Art Unit	2824
Examiner Name	LE, Vu Ang
Attorney Docket Number	001701.00676

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP3414587	04/04/03			Abstract

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

Abstract (Basic): JP 9326199 A

The memory has a memory cell array (100) in which multiple non-volatile memory cells are configured. A bit-line is connected with the current flow path of the memory cell array and the word line is connected with the control gate of the cell array. Multiple sense latch circuits (110,120) and a bypass circuit (170) for the potential holder are connected with the bit-line of the memory cell array. Based on the predetermined data stored in the latch circuit, the data written-in the memory cell is checked for normal data write- in operation. When the threshold value of the data in the memory cell is less than the predetermined value, the potential of the bit-line from the bypass circuit is increased to high level by a voltage switching circuit (160). When the threshold value of the data is more than the predetermined value, then the potential value to the bit-line is released. ADVANTAGE - Enables data write-in operation control by threshold value adjustment. Shortens data write-in time in memory cell.

Dwg.2/21

Title Terms: ELECTRIC; ERASE; NON; VOLATILE; SEMICONDUCTOR; MEMORY; EEPROM; PORTABLE; TELEPHONE; PAGE; VOLTAGE; SWITCH; CIRCUIT; CONTROL; POTENTIAL; LEVEL; SUPPLY; BIT; LINE; CIRCUIT; BASED; THRESHOLD; VOLTAGE; LEVEL; DATA; WRITING; MEMORY; CELL
Derwent Class: U13; U14
International Patent Class (Main): G11C-016/02; G11C-016/06
File Segment: EPI
Manual Codes (EPI/S-X): U13-C04B2; U14-A03B7; U14-A07B

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